Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A high voltage selecting circuit comprising:
a first transistor where a first terminal of the first transistor being electrically coupled to a first voltage, a second terminal of the first transistor being electrically coupled to an output node, and a gate of the first transistor being electrically coupled to a second voltage; and
a second transistor where a first terminal of the second transistor being electrically coupled to the second voltage, a second terminal of the second transistor being electrically coupled to the output node, and a gate of the second transistor being electrically coupled to the first voltage;
wherein the high voltage selecting circuit selectively generates an output voltage according to a higher one of the first voltage and the second voltage.

[c2] 2. The high voltage selecting circuit in claim 1, wherein the first transistor is a p-type MOS transistor and the first terminal of the first transistor is a source and the second terminal of the first transistor is a drain.

[c3] 3. The high voltage selecting circuit in claim 1, wherein

the second transistor is a p-type MOS transistor and the first terminal of the second transistor is a source and the second terminal of the second transistor is a drain.

[c4] 4. The high voltage selecting circuit in claim 1, wherein the first transistor further comprising a well and the well is electrically coupled to the second terminal of the first transistor.

[c5] 5. The high voltage selecting circuit in claim 1, wherein the second transistor further comprising a well and the well is electrically coupled to the second terminal of the second transistor.

[c6] 6. The high voltage selecting circuit in claim 1, wherein an absolute value of a difference between the first voltage and the second voltage is larger than a threshold voltage of the transistors, and the output voltage is substantially a higher one of the first voltage and the second voltage.

[c7] 7. The high voltage selecting circuit in claim 1, wherein an absolute value of a difference between the first voltage and the second voltage is smaller than a threshold voltage of the transistors and the output voltage is substantially the higher one of the first voltage and the second voltage subtracting an junction voltage between the

first terminal and the well of the transistor.

[c8] 8. A power supply voltage switching circuit for selecting a power supply voltage for an integrated circuit according to a first control signal, the circuit comprising:
a high voltage selecting module for generating an output voltage according to a higher one of a first voltage and a second voltage;
a level shifting module electrically coupled to the high voltage selecting module for inputting the output voltage as a power supply of the level shifting module, for performing level shift on the first control signal according to the output voltage; and
a selecting switch module electrically coupled to the level shifting module, for selectively outputting the first voltage or the second voltage as the power supply voltage of the integrated circuit according to the level-shifted first control signal.

[c9] 9. The circuit in claim 8, wherein the high voltage selecting module comprises:
a first transistor where a first terminal of the first transistor being electrically coupled to a first voltage, a second terminal of the first transistor being electrically coupled to an output node, and a gate of the first transistor being electrically coupled to a second voltage; and
a second transistor where a first terminal of the second

transistor being electrically coupled to the second voltage, a second terminal of the second transistor being electrically coupled to the output node, and a gate of the second transistor being electrically coupled to the first voltage;

wherein the high voltage selecting module selectively generates an output voltage according to a higher one of the first voltage and the second voltage.

[c10] 10. The circuit in claim 9, wherein the first transistor is a p-type MOS transistor and the first terminal of the first transistor is a source and the second terminal of the first transistor is a drain.

[c11] 11. The circuit in claim 9, wherein the second transistor is a p-type MOS transistor and the first terminal of the second transistor is a source and the second terminal of the second transistor is a drain.

[c12] 12. The circuit in claim 9, wherein the first transistor further comprises a well and the well is electrically coupled to the second terminal of the first transistor.

[c13] 13. The circuit in claim 9, wherein the second transistor further comprises a well and the well is electrically coupled to the second terminal of the second transistor.

[c14] 14. The circuit in claim 9, wherein an absolute value of a

difference between the first voltage and the second voltage is larger than a threshold voltage of the transistors and the output voltage is substantially the higher one of the first voltage and the second voltage.

[c15] 15. The circuit in claim 9, wherein an absolute value of a difference between the first voltage and the second voltage is smaller than a threshold voltage of the transistors and the output voltage is substantially the higher one of the first voltage and the second voltage subtracting an junction voltage between the first terminal and the well of the transistor.

[c16] 16. The circuit in claim 8, wherein the level shifting module further performs level shift on a second control signal according to the output voltage and the second control signal is complementary to the first control signal.

[c17] 17. The circuit in claim 16, wherein the selecting switch module further comprises:
a third transistor where a first terminal of the third transistor being electrically coupled to the first voltage, a second terminal of the third transistor being electrically coupled to a supply node, and the gate of the third transistor being electrically coupled to the level-shifted first control signal; and

a fourth transistor where a first terminal of the fourth transistor being electrically coupled to the second voltage, a second terminal of the fourth transistor being electrically coupled to the supply node, and a gate of the fourth transistor being electrically coupled to the level-shifted second control signal;
wherein the selecting switch module generates the power supply voltage for the integrated circuit at the supply node according to the level-shifted first and second control voltage.

[c18] 18. The circuit in claim 17, wherein the third transistor is a p-type MOS transistor and the first terminal of the third transistor is a source and the second terminal of the third transistor is a drain.

[c19] 19. The circuit in claim 17, wherein the fourth transistor is a p-type MOS transistor and the first terminal of the fourth transistor is a source and the second terminal of the fourth transistor is a drain.